ABSTRACT OF THE DISCLOSURE

A device and method are provided for testing the timing of an output signal from a circuit. The output signal can be sent from a circuit contained within a portion of an integrated circuit, and represents a response to a test pattern or stimuli applied to that circuit. The output signal is compared to an expected output signal to determine skew of that signal relative to the clocking of the circuit. Testing the output signal involves placing a characterization path within the functional path of the output signal, between the circuits being tested and an output terminal that can receive a measurement device. By placing the characterization path into the functional path, the output signal sees only a single load gate terminal of, for example, a logic gate. The reduced loading not only positively impacts the normal operation of the output signal, but also beneficially minimizes the possibility of any inaccuracies in the characterization testing.